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09/684,287	10/06/2000	Steven A. Brosey	80113-0103	1440

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EXAMINER
BUI, KIEU OANH T

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 04/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 09/684,287	**Applicant(s)** BROSEY, STEVEN A.
	Examiner KIEU-OANH T BUI	**Art Unit** 2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-35* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-35* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7&8*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless --*
> *(b) the invention was patented or described in a printed publication in this or a foreign country or in public*
> *use or on sale in this country, more than one year prior to the date of application for patent in the United*
> *States.*

2.   Claims 1-13, and 17-35 are rejected under 35 U.S.C. 102(b) as being anticipated by

Blatter et al. (U.S. Patent No. 5,754,651/ or "Blatter" hereinafter).

Regarding claim 1, Blatter discloses "an apparatus for extracting messages from a digital

data stream containing messages", i.e., an apparatus as shown in Fig. 1 for extracting messages

from a digital data stream MPEG (col. 1/lines 18-47 for MPEG; and col. 2/lines 49-60 for

extracting messages from the stream), comprising: "a message processor that receives the digital

data stream and extracts message portions from the digital data stream", i.e., a decoder 55

receives and extracts message portions from the digital stream to buffers (col. 6/lines 23-42); "a

first buffer having a plurality of locations associated with a plurality of channels to store the

extracted message portions; and a second buffer having a plurality of locations associated with

the plurality of channels for storing state data corresponding to the extracted message portions",

i.e., buffer 60 has more than 2 buffers for storing the program or extract message portions and

including the PSI information regarding as "state data" for information corresponding to the

extracted message portions (col. 6/lines 23-42 & col. 2/lines 25-60 for PSI information

addressed).

As for claim 2, in further view of claim 1 above, Blatter further discloses "comprising a

central processing unit interface for coupling the apparatus to a central processing unit", i.e., a

buffer control interface 65 acts as an interface for the apparatus coupled to system controller 115

(Fig. 1 and col. 4/lines 23-43).

Regarding claim 3, Blatter discloses "a device for extracting messages from a data

stream", i.e., an apparatus as shown in Fig. 1 for extracting messages from a digital data stream

MPEG (col. 1/lines 18-47 for MPEG; and col. 2/lines 49-60 for extracting messages from the

stream) comprising: "an input interface that receives packet data in the data stream", i.e., a

decoder 30 acts as an input interface for receiving packet data in the data stream (Fig. 1, and col.

3/lines 38-60); "a packet identifier filter coupled to the input interface to selectively filter the

packet data" (Fig. 1/unit 45 for a PID filter, and col. 4/lines 44-65), "the packet identifier filter

having a central processing unit (CPU) interface to allow communication between the device and

a CPU", i.e., a buffer control interface 65 acts as a CPU interface for allowing communication

between the device and the system controller 115 (Fig. 1); "a message processor that receives the

selectively filtered packet data from the packet identifier filter and extracts message portions

from the packet data", i.e., a decoder 55 receives and extracts message portions from the digital

stream to buffers (col. 6/lines 23-42); "a first buffer having a plurality of locations associated

with a plurality of channels to store the extracted message portions; and a second buffer having a

plurality of locations associated with the plurality of channels for storing state data

corresponding to the extracted message portions", i.e., buffer 60 has more than 2 buffers for

storing the program or extract message portions and including the PSI information regarding as

"state data" for information corresponding to the extracted message portions (col. 6/lines 23-42

& col. 2/lines 25-60 for PSI information addressed).

As for claim 4, in further view of claim 3, Blatter further shows "wherein the input

interface converts the packet data into parallel packet data", i.e., the CPSI stream can be

separated and stored in two parallel helical and non-helical tracks as parallel packet data (col.

14/lines 3-36).

As for claim 5, in further view of claim 4, Blatter further discloses "wherein the parallel

packet data is sent to the packet identifier filter with a enable signal to validate byte data in the

packet", i.e., the PIDs of the programs are provided to packet identifier filter to enable the

validation or identifying packets for selected programs (col. 7/lines 38-50).

As for claim 6, in further view of claim 5, Blatter further discloses "wherein the input

interface generates at least one clock enable signal to resynchronize the byte data" (col. 5/line 57

to col. 6/line 22 for a program clock reference for synchronizing and decoding of content packets

after the input interface receives the content packets).

As for claim 7, in further view of claim 3, Blatter further suggests "wherein the packet

identifier filter provides at least one selected from the group consisting of mode control, filtering

control, enable control and masking control for each channel in the message processor" (Fig. 2

shows a process to generate CPSI from PSI and to incorporate the CPSI in a packetized

datastream suitable for storage on a selectable storage medium is an example for the packet

identifier filter provides at least one selected from the group consisting of mode control, filtering

control, enable control and masking control for each channel in the message processor, see col.

6/line 23 to col. 8/line 3).

As for claim 8, in further view of claim 7 above, Blatter further shows "wherein the mode

control includes selecting one of a plurality of storage modes, each storage mode corresponding

to a buffer size for the first buffer", i.e., based upon a destination flag, the control unit determines

which one is for which appropriate buffer size according to video, data or audio (col. 5/lines 35-

56 & col. 6/lines 23-60).

As for claim 9, in further view of claim 7 above, Blatter further mentions "wherein the

mode control includes selecting one of a capture mode, where the packet data is stored in the first

buffer as a full packet without a sync byte, and a message mode, where messages in the packet

data are allowed to be processed" (col. 7/lines 28-37 & col.7/line 50 to col. 8/line 3 for full

program specific information (PSI) being captured and data in the packet data are processed

whether in an encryption form or not to appropriate storage).

As for claim 10, in further view of claim 7 above, Blatter further mentions "wherein the

filtering control includes selecting whether address filtering is turned on or off, and wherein all

messages in the packet data are processed when the address filtering is turned on and selected

messages in the packet data are processed when the address filtering is turned off", i.e., all the

message data is filtering", i.e., whether there is a need for an NRSS decryption, a switch at 35

provides as an on/off switch for the unit 45 decode PID selection as a PID filter also by matching

with pre-stored PID selection in unit 47 during the message address filtering process (Fig. 1, and

col. 4/line 23 to col. 5/line 22).

As for claim 11, in further view of claim 3 and 10 above, Blatter inherently discloses

"wherein the filter module has a pipeline delay to allow the packet identifier of an incoming

packet to be compared with at least one predetermined packet identifier", i.e., a pre-stored PID is

compared and matched during the filtering process above, suggesting to include a pipeline delay

(Fig. 1, and col. 4/line 23 to col. 5/line 22).

As for claim 12, in further view of claim 3 above, Blatter further discloses "wherein the

filter module validates the incoming packet by checking a header in the incoming packet with at

least one predetermined condition" (col. 4/lines 44-58 as header information is checked whether

at least one predetermined condition as encryption or not is addressed).

As for claim 13, in further view of claim 3, Blatter shows "wherein the message

processor conducts a first process to find a start of a new message in the packet data and a

second process to extract and store the message", i.e., a header of the new message is detected

and then being extracted and stored the message in later steps (col. 4/lines 22-58, and col. 5/lines

35-56).

As for claim 17, in further view of claim 3, Blatter shows "wherein the message

processor includes: a processor state machine shared between the plurality of channels, wherein

the state data from the processor state machine is stored in the second buffer; an address filter

control circuit; and a verification circuit that calculates a verification code and compares the

calculated verification code with an embedded verification code in the message portion in the

packet data", i.e., PSI data as state date and being stored in a different buffer (col. 4/lines 22-58

& col. 6/lines 23-42); a PID filter and a verification circuit in comparing the PID with the pre-

stored PID in the message are addressed earlier claims above.

As for claim 18, in further view of claim 17, Blatter suggests "wherein the message

processor further includes an alternative packet capture control that stops message processing for

a single channel and captures a single packet for storage in the first buffer" (col. 7/lines 25-37 for

the capture of PSI packets during the PSI interruption).

As for claim 19, in further view of claim 17, Blatter further shows "further comprising a

buffer control that controls CPU operation while the at least one of the first and second buffers is

being read" (Fig. 1 for unit 65 for a buffer control, and col. 5/lines 35-56).

As for claim 20, in further view of claim 19, Blatter further shows "comprising a message

ready interrupt control coupled to the buffer control, wherein the message ready interrupt control

generates signals for determining which channels have messages that are ready for processing

when the CPU is interrupted based on state data in the second buffer", i.e., a PSI generator

system controller 115 provides PSI interruption to the buffer control and generates control

signals for determining which channels have messages for processing (col. 6/lines 9-60).

As for claims 21-23, these claims comprising "a message error interface for identifying

the presence of lost messages"; "wherein the message error interface includes a first error circuit

that identifies messages lost due to corrupt packets and a second error circuit that identifies

messages lost due to first buffer overflow"; and "wherein the first and second error circuits are

provided for each one of said plurality of channels" are met (col. 14/lines 3-16 as known error

encoding, and col. 10/line 52 to col. 11/line 22 for error detection technique including overflow

and col. 15/line 49 to col. 16/line 5 for discontinuity or mismatch between packets of a PID and

transport error indications addressed).

Regarding claims 24-35, these claims for "a method for extracting messages from a data stream, comprising: receiving packet data in the data stream; selectively filtering the packet data; extracting at least a portion of a message from the packet data; storing said at least a portion of the message in a first buffer associated with said message processor; and storing state data corresponding with said at least a portion of the message in a second buffer" are rejected for the reasons given in the scope of claims 1-13 and 17-23 as discussed in details above.

Claim Rejections - 35 USC 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

4.   Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blatter et al. (U.S. Patent No. 5,754,651).

Regarding claims 14-16, in further view of claim 3, Blatter does not show "wherein the first buffers are circular buffers"; "wherein the first buffer includes 32 available channels each with a 2K buffer for message storage" and "wherein the first buffer includes 16 channels with a 2K buffer and 4 channels with an 8K buffer for message storage"; however, the Examiner takes an Official Notice that it is simply a design choice of the system whether to allocate any buffer type or buffer size for message storage depending on the size of the system and the need for storage. It really does not construct any novelty in whether some one uses this type of buffer or another with this much capacity for a number of channels with a 2K or 8K or 100K for message storage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Blatter's system with some detailed of the buffer type and the buffer size in order to simply specify the allocation of buffers for message storage within the system.

Conclusion

5.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Blatter et al. (US. Pat. No.5,844,595) disclose a decoding of digital data including program specific information.

Blatter et al. (US. Pat. No.5,838,873) disclose packetized data formats for digital data storage media.

Hamery et al. (US Pat. No.6,650,710 B1) disclose a packet filtering.

Komi et al. (US. Pat. No.6,477,185 B1) disclose a demultiplexing and decoding apparatus for coded audio and video data.

Fries (US Pat. No.6,317,885 B1) discloses an interactive entertainment and information system using television set-top-box.

Loukianov (US Pat. No.6,249,526 B1) discloses a verdatile time division multiple access slot assignment unit.

Wakeland (US Pat. No.6,101,192) discloses a network router with partitioned memory for optimized data storage and retrieval.

Berg et al. (US Pat. No.6,680,952 B1) disclose a method and apparatus for backhaul of

telecommunications signaling protocols over packet switching networks.

6.   **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9306, (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

7.   Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Krista Kieu-Oanh Bui whose telephone number is (703) 305-0095. The

examiner can normally be reached on Monday-Friday from 9:00 AM to 6:30 PM, with alternate

Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Andrew Faile, can be reached on (703) 305-4380.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to Technology Center 2600 Customer Service Office whose telephone number

is (703) 306-0377.

Krista Bui
Art Unit 2611
April 8, 2004

KRISTA BUI
PATENT EXAMINER